

**Translation**

**PATENT COOPERATION TREATY**

**PCT**

**INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY**  
(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference <b>13225 Ko/tp</b>	FOR FURTHER ACTION See Form PCT/IPEA/416	
International application No. <b>PCT/DE2004/001588</b>	International filing date (day/month/year) <b>21.07.2004</b>	Priority date (day/month/year) <b>23.07.2003</b>
International Patent Classification (IPC) or national classification and IPC <b>H01L21/28, H01L21/336, H01L21/8246, H01L29/792, H01L27/115, H01L51/30</b>		
Applicant <b>INFINEON TECHNOLOGIES AG</b>		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

3. This report is also accompanied by ANNEXES, comprising:

a. ☒ (sent to the applicant and to the International Bureau) a total of 6 sheets, as follows:

☒ sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).

☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

b. ☐ (sent to the International Bureau only) a total of \_\_\_\_\_, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

<input checked="" type="checkbox"/>	Box No. I	Basis of the report
<input type="checkbox"/>	Box No. II	Priority
<input type="checkbox"/>	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
<input type="checkbox"/>	Box No. IV	Lack of unity of invention
<input checked="" type="checkbox"/>	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
<input type="checkbox"/>	Box No. VI	Certain documents cited
<input type="checkbox"/>	Box No. VII	Certain defects in the international application
<input type="checkbox"/>	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
Name and mailing address of the IPEA/EP	Authorized officer
Facsimile No.	Telephone No.

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## Box No. I Basis of the report

1. With regard to the language, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.
- ☐ This report is based on translations from the original language into the following language \_\_\_\_\_, which is the language of a translation furnished for the purposes of:
- ☐ international search (Rule 12.3 and 23.1(b))
- ☐ publication of the international application (Rule 12.4)
- ☐ international preliminary examination (Rule 55.2 and/or 55.3)
2. With regard to the elements of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:
- ☐ the international application as originally filed/furnished
- ☒ the description:
- pages 1-20 \_\_\_\_\_ as originally filed/furnished
- pages\* \_\_\_\_\_ received by this Authority on \_\_\_\_\_
- pages\* \_\_\_\_\_ received by this Authority on \_\_\_\_\_
- ☒ the claims:
- nos. \_\_\_\_\_ as originally filed/furnished
- nos.\* \_\_\_\_\_ as amended (together with any statement) under Article 19
- nos.\* 1-22 \_\_\_\_\_ received by this Authority on 13.05.2005 with letter of 13.05.2005
- nos.\* \_\_\_\_\_ received by this Authority on \_\_\_\_\_
- ☒ the drawings:
- sheets 1/5-5/5 \_\_\_\_\_ as originally filed/furnished
- sheets\* \_\_\_\_\_ received by this Authority on \_\_\_\_\_
- sheets\* \_\_\_\_\_ received by this Authority on \_\_\_\_\_
- ☐ a sequence listing and/or any related table(s) – see Supplemental Box Relating to Sequence Listing.
3. ☐ The amendments have resulted in the cancellation of:
- ☐ the description, pages \_\_\_\_\_
- ☐ the claims, nos. \_\_\_\_\_
- ☐ the drawings, sheets/figs \_\_\_\_\_
- ☐ the sequence listing (*specify*): \_\_\_\_\_
- ☐ any table(s) related to sequence listing (*specify*): \_\_\_\_\_
4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
- ☐ the description, pages \_\_\_\_\_
- ☐ the claims, nos. \_\_\_\_\_
- ☐ the drawings, sheets/figs \_\_\_\_\_
- ☐ the sequence listing (*specify*): \_\_\_\_\_
- ☐ any table(s) related to sequence listing (*specify*): \_\_\_\_\_

\* If item 4 applies, some or all of those sheets may be marked "superseded."

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Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement		
1. Statement			
Novelty (N)	Claims	<u>1-22</u>	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	<u>1-22</u>	NO
Industrial applicability (IA)	Claims	<u>1-22</u>	YES
	Claims		NO
2. Citations and explanations (Rule 70.7)			
1. This report makes reference to the following documents:			
D1: US-A-6 051 467 (CHA CHER LIANG ET AL) 18 April 2000 (2000-04-18)			
D2: JUNG DAL CHOI ET AL: "A triple polysilicon stacked flash memory cell with wordline self- boosting programming" ELECTRON DEVICES MEETING, 1997. TECHNICAL DIGEST., INTERNATIONAL, WASHINGTON, DC, USA 7-10 DEC. 1997, NEW YORK, NY, USA, IEEE, US, 7 December 1997 (1997-12-07), pages 283-286, XP010265507 ISBN: 0-7803-4100-7			
D3: US 2003/111670 A1 (KUHR WERNER G ET AL) 19 June 2003 (2003-06-19)			
D4: US 2002/015322 A1 (CLOUD EUGENE H ET AL) 7 February 2002 (2002-02-07)			
D5: US-A-5 981 335 (CHI MIN-HWA) 9 November 1999 (1999-11-09)			
2. The application fails to meet the requirements of PCT Article 33(1) and (3) (inventive step).			
2.1 D1 (see column 1, line 57 to column 4, line 57;			

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paragraphs 1-11) is considered to be the closest prior art and discloses a method of producing a memory device having semiconductor structures and memory cells, said method having the following steps:

- a) production of a transistor having source/drain regions (26) and a gate dielectric (16) over the channel region;
- b) production of a first gate electrode (18) on the gate dielectric (16);
- c) completion "of processing of the semiconductor structures" from steps a) and b) by depositing and polishing an oxide layer (30);
- d) production of a storage layer (36) which is connected to the first gate electrode (18) by means of a conductive compound (32);
- e) production of an insulating layer (50, 54) over the storage layer (36).

Thus D1 and the subject matter of claims 1 and 11 differ in that, in the claims, a "second gate electrode" is provided over the storage layer, it being assumed that a gate electrode is characterized by the fact that it is connected in a non-conductive manner to the structure with respect to which it is intended to act as a gate (and the electrode 52 in D1 is therefore not regarded as such a gate electrode).

The objective technical problem to be solved is therefore that of making it possible to operate

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the memory device with the lowest possible voltages.

D2 discloses a method of improving a memory cell as known from D1 in such a way that the programming voltages are significantly reduced by using a "booster gate" electrode, which corresponds to the "second gate electrode" of the present application. This method is of interest to a person skilled in the art because the power consumption is thereby reduced. A person skilled in the art would therefore combine the teachings of D1 and D2 in order to provide an improved memory device.

The subject matter of independent claims 1 and 11 is therefore not inventive in relation to a combination of D1 and D2.

2.2 For the sake of completeness, the following should be noted.

An ONO layer *per se* (see layer 36 in D1) is generally known as a storage layer, i.e. electrical charges can be stored in an ONO layer. Whether, in a memory cell, the charge is in fact stored in the ONO layer or in another layer depends on the electrical voltages that are applied to or present at various points of the cell during use of the cell.

Claims 1 and 11 of the present application define

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a layer structure and a method of producing the same, which method is also obvious from a combination of D1 and D2 (see point 2.1 above). The structure described in the claims does not, however, allow any conclusions to be made regarding the use thereof. For example, it is not clear from claims 1 and 11 whether or not the "first gate electrode" is/can be a floating gate (as known from D1); thus *inter alia* a floating gate falls under the scope of protection.

3. The remaining claims do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of PCT Article 33 for novelty and inventive step (see D1 to D5 and the corresponding passages in the search report).

Claims 2-3, 6, 12-13, 16 and 20 are disclosed in D1.

Claims 4-5, 7, 10, 14-15, 17 and 21-22: generally known features.

Claims 8-9 and 18-19: D3 discloses that storage layers are advantageously made of porphyrin molecules, and also discloses that, in the production process, all high-temperature steps must be carried out prior to deposition of the porphyrin molecules.

4. The application fails to meet the requirements of

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PCT Article 6 (clarity).

The description, page 5, lines 1-19, and page 6, lines 8-18, suggests that the following features are essential to the definition of the invention:

- (1) the storage layer is deposited only after completion of the process steps that require high temperatures;
- (2) the storage layer consists of an organic layer.

Since independent claims 1, 11 and 22 do not contain these features, these claims fail to meet the requirement of PCT Article 6 in conjunction with PCT Rule 6.3(b) that each independent claim must include all the technical features essential to the definition of the invention.

It should be noted that the feature of the storage layer being applied in a spatially separate manner with regard to the actual transistor region is not sufficient for describing the feature (1) above.